Armondo Thomas

Partner: Grant Swenson

EE 310

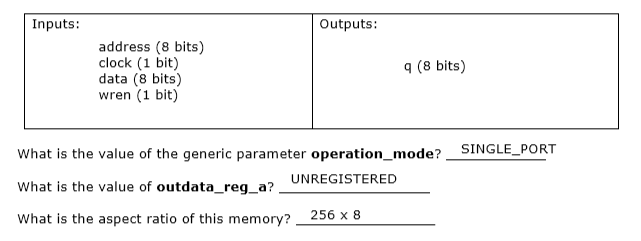
April 4, 2017

# Lab 6: Memory Report

## Introduction

We implemented a memory module on the FPGA board.

## Activity 1



### VHDL Code

-- megafunction wizard: %RAM: 1-PORT%

-- GENERATION: STANDARD

-- VERSION: WM1.0

-- MODULE: altsyncram

-- ============================================================

-- File Name: ramlpm.vhd

-- Megafunction Name(s):

-- altsyncram

--

-- Simulation Library Files(s):

-- altera\_mf

-- ============================================================

-- \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

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--authorized distributors. Please refer to the applicable

--agreement for further details.

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

LIBRARY altera\_mf;

USE altera\_mf.altera\_mf\_components.all;

ENTITY ramlpm IS

PORT

(

address : IN STD\_LOGIC\_VECTOR (7 DOWNTO 0);

clock : IN STD\_LOGIC := '1';

data : IN STD\_LOGIC\_VECTOR (7 DOWNTO 0);

wren : IN STD\_LOGIC ;

q : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0)

);

END ramlpm;

ARCHITECTURE SYN OF ramlpm IS

SIGNAL sub\_wire0 : STD\_LOGIC\_VECTOR (7 DOWNTO 0);

BEGIN

q <= sub\_wire0(7 DOWNTO 0);

altsyncram\_component : altsyncram

GENERIC MAP (

clock\_enable\_input\_a => "BYPASS",

clock\_enable\_output\_a => "BYPASS",

intended\_device\_family => "Cyclone V",

lpm\_hint => "ENABLE\_RUNTIME\_MOD=NO",

lpm\_type => "altsyncram",

numwords\_a => 256,

operation\_mode => "SINGLE\_PORT",

outdata\_aclr\_a => "NONE",

outdata\_reg\_a => "UNREGISTERED",

power\_up\_uninitialized => "FALSE",

ram\_block\_type => "M10K",

read\_during\_write\_mode\_port\_a => "NEW\_DATA\_NO\_NBE\_READ",

widthad\_a => 8,

width\_a => 8,

width\_byteena\_a => 1

)

PORT MAP (

address\_a => address,

clock0 => clock,

data\_a => data,

wren\_a => wren,

q\_a => sub\_wire0

);

END SYN;

-- ============================================================

-- CNX file retrieval info

-- ============================================================

-- Retrieval info: PRIVATE: ADDRESSSTALL\_A NUMERIC "0"

-- Retrieval info: PRIVATE: AclrAddr NUMERIC "0"

-- Retrieval info: PRIVATE: AclrByte NUMERIC "0"

-- Retrieval info: PRIVATE: AclrData NUMERIC "0"

-- Retrieval info: PRIVATE: AclrOutput NUMERIC "0"

-- Retrieval info: PRIVATE: BYTE\_ENABLE NUMERIC "0"

-- Retrieval info: PRIVATE: BYTE\_SIZE NUMERIC "8"

-- Retrieval info: PRIVATE: BlankMemory NUMERIC "1"

-- Retrieval info: PRIVATE: CLOCK\_ENABLE\_INPUT\_A NUMERIC "0"

-- Retrieval info: PRIVATE: CLOCK\_ENABLE\_OUTPUT\_A NUMERIC "0"

-- Retrieval info: PRIVATE: Clken NUMERIC "0"

-- Retrieval info: PRIVATE: DataBusSeparated NUMERIC "1"

-- Retrieval info: PRIVATE: IMPLEMENT\_IN\_LES NUMERIC "0"

-- Retrieval info: PRIVATE: INIT\_FILE\_LAYOUT STRING "PORT\_A"

-- Retrieval info: PRIVATE: INIT\_TO\_SIM\_X NUMERIC "0"

-- Retrieval info: PRIVATE: INTENDED\_DEVICE\_FAMILY STRING "Cyclone V"

-- Retrieval info: PRIVATE: JTAG\_ENABLED NUMERIC "0"

-- Retrieval info: PRIVATE: JTAG\_ID STRING "NONE"

-- Retrieval info: PRIVATE: MAXIMUM\_DEPTH NUMERIC "0"

-- Retrieval info: PRIVATE: MIFfilename STRING ""

-- Retrieval info: PRIVATE: NUMWORDS\_A NUMERIC "256"

-- Retrieval info: PRIVATE: RAM\_BLOCK\_TYPE NUMERIC "2"

-- Retrieval info: PRIVATE: READ\_DURING\_WRITE\_MODE\_PORT\_A NUMERIC "3"

-- Retrieval info: PRIVATE: RegAddr NUMERIC "1"

-- Retrieval info: PRIVATE: RegData NUMERIC "1"

-- Retrieval info: PRIVATE: RegOutput NUMERIC "0"

-- Retrieval info: PRIVATE: SYNTH\_WRAPPER\_GEN\_POSTFIX STRING "0"

-- Retrieval info: PRIVATE: SingleClock NUMERIC "1"

-- Retrieval info: PRIVATE: UseDQRAM NUMERIC "1"

-- Retrieval info: PRIVATE: WRCONTROL\_ACLR\_A NUMERIC "0"

-- Retrieval info: PRIVATE: WidthAddr NUMERIC "8"

-- Retrieval info: PRIVATE: WidthData NUMERIC "8"

-- Retrieval info: PRIVATE: rden NUMERIC "0"

-- Retrieval info: LIBRARY: altera\_mf altera\_mf.altera\_mf\_components.all

-- Retrieval info: CONSTANT: CLOCK\_ENABLE\_INPUT\_A STRING "BYPASS"

-- Retrieval info: CONSTANT: CLOCK\_ENABLE\_OUTPUT\_A STRING "BYPASS"

-- Retrieval info: CONSTANT: INTENDED\_DEVICE\_FAMILY STRING "Cyclone V"

-- Retrieval info: CONSTANT: LPM\_HINT STRING "ENABLE\_RUNTIME\_MOD=NO"

-- Retrieval info: CONSTANT: LPM\_TYPE STRING "altsyncram"

-- Retrieval info: CONSTANT: NUMWORDS\_A NUMERIC "256"

-- Retrieval info: CONSTANT: OPERATION\_MODE STRING "SINGLE\_PORT"

-- Retrieval info: CONSTANT: OUTDATA\_ACLR\_A STRING "NONE"

-- Retrieval info: CONSTANT: OUTDATA\_REG\_A STRING "UNREGISTERED"

-- Retrieval info: CONSTANT: POWER\_UP\_UNINITIALIZED STRING "FALSE"

-- Retrieval info: CONSTANT: RAM\_BLOCK\_TYPE STRING "M10K"

-- Retrieval info: CONSTANT: READ\_DURING\_WRITE\_MODE\_PORT\_A STRING "NEW\_DATA\_NO\_NBE\_READ"

-- Retrieval info: CONSTANT: WIDTHAD\_A NUMERIC "8"

-- Retrieval info: CONSTANT: WIDTH\_A NUMERIC "8"

-- Retrieval info: CONSTANT: WIDTH\_BYTEENA\_A NUMERIC "1"

-- Retrieval info: USED\_PORT: address 0 0 8 0 INPUT NODEFVAL "address[7..0]"

-- Retrieval info: USED\_PORT: clock 0 0 0 0 INPUT VCC "clock"

-- Retrieval info: USED\_PORT: data 0 0 8 0 INPUT NODEFVAL "data[7..0]"

-- Retrieval info: USED\_PORT: q 0 0 8 0 OUTPUT NODEFVAL "q[7..0]"

-- Retrieval info: USED\_PORT: wren 0 0 0 0 INPUT NODEFVAL "wren"

-- Retrieval info: CONNECT: @address\_a 0 0 8 0 address 0 0 8 0

-- Retrieval info: CONNECT: @clock0 0 0 0 0 clock 0 0 0 0

-- Retrieval info: CONNECT: @data\_a 0 0 8 0 data 0 0 8 0

-- Retrieval info: CONNECT: @wren\_a 0 0 0 0 wren 0 0 0 0

-- Retrieval info: CONNECT: q 0 0 8 0 @q\_a 0 0 8 0

-- Retrieval info: GEN\_FILE: TYPE\_NORMAL ramlpm.vhd TRUE

-- Retrieval info: GEN\_FILE: TYPE\_NORMAL ramlpm.inc FALSE

-- Retrieval info: GEN\_FILE: TYPE\_NORMAL ramlpm.cmp TRUE

-- Retrieval info: GEN\_FILE: TYPE\_NORMAL ramlpm.bsf TRUE

-- Retrieval info: GEN\_FILE: TYPE\_NORMAL ramlpm\_inst.vhd TRUE

-- Retrieval info: LIB\_FILE: altera\_mf

### Do Code

**Part 1: Read first 16 addresses’ initial data**

add wave -in \*

add wave -out \*

restart -f

force clock 0 0ns, 1 50ns -r 100ns;

force data(7 downto 0) "11111111";

force wren 0;

force address(0) 0 0ns, 1 100ns -r 200ns;

force address(1) 0 0ns, 1 200ns -r 400ns;

force address(2) 0 0ns, 1 400ns -r 800ns;

force address(3) 0 0ns, 1 800ns -r 1600ns;

force address(7 downto 4) "0000";

run 1600ns;

**Part 2: Testing read/write**

add wave -in \*

add wave -out \*

restart -f

force wren 1

force clk 0 0ns, 1 20ns -r 40ns

force address x"00"

force data x"0F"

run 40ns

force address x"01"

force data x"1E"

run 40ns

force address x"02"

force data x"2D"

run 40ns

force address x"03"

force data x"3C"

run 40ns

force address x"04"

force data x"4B"

run 40ns

force address x"05"

force data x"5A"

run 40ns

force address x"06"

force data x"69"

run 40ns

force address x"07"

force data x"78"

run 40ns

force address x"08"

force data x"87"

run 40ns

force address x"09"

force data x"96"

run 40ns

force address x"0A"

force data x"A5"

run 40ns

force address x"0B"

force data x"B4"

run 40ns

force address x"0C"

force data x"C3"

run 40ns

force address x"0D"

force data x"D2"

run 40ns

force address x"0E"

force data x"E1"

run 40ns

force address x"0F"

force data x"F0"

run 40ns

## Activity 2

### VHDL Code

**ramplminit.vhd**

-- megafunction wizard: %RAM: 1-PORT%

-- GENERATION: STANDARD

-- VERSION: WM1.0

-- MODULE: altsyncram

-- ============================================================

-- File Name: ramlpminit.vhd

-- Megafunction Name(s):

-- altsyncram

--

-- Simulation Library Files(s):

-- altera\_mf

-- ============================================================

-- \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

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--the Altera MegaCore Function License Agreement, or other

--applicable license agreement, including, without limitation,

--that your use is for the sole purpose of programming logic

--devices manufactured by Altera and sold by Altera or its

--authorized distributors. Please refer to the applicable

--agreement for further details.

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

LIBRARY altera\_mf;

USE altera\_mf.altera\_mf\_components.all;

ENTITY ramlpminit IS

PORT

(

address : IN STD\_LOGIC\_VECTOR (7 DOWNTO 0);

clock : IN STD\_LOGIC := '1';

data : IN STD\_LOGIC\_VECTOR (7 DOWNTO 0);

wren : IN STD\_LOGIC ;

q : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0)

);

END ramlpminit;

ARCHITECTURE SYN OF ramlpminit IS

SIGNAL sub\_wire0 : STD\_LOGIC\_VECTOR (7 DOWNTO 0);

BEGIN

q <= sub\_wire0(7 DOWNTO 0);

altsyncram\_component : altsyncram

GENERIC MAP (

clock\_enable\_input\_a => "BYPASS",

clock\_enable\_output\_a => "BYPASS",

init\_file => "ramlpminit.mif",

intended\_device\_family => "Cyclone V",

lpm\_hint => "ENABLE\_RUNTIME\_MOD=NO",

lpm\_type => "altsyncram",

numwords\_a => 256,

operation\_mode => "SINGLE\_PORT",

outdata\_aclr\_a => "NONE",

outdata\_reg\_a => "UNREGISTERED",

power\_up\_uninitialized => "FALSE",

read\_during\_write\_mode\_port\_a => "NEW\_DATA\_NO\_NBE\_READ",

widthad\_a => 8,

width\_a => 8,

width\_byteena\_a => 1

)

PORT MAP (

address\_a => address,

clock0 => clock,

data\_a => data,

wren\_a => wren,

q\_a => sub\_wire0

);

END SYN;

-- ============================================================

-- CNX file retrieval info

-- ============================================================

-- Retrieval info: PRIVATE: ADDRESSSTALL\_A NUMERIC "0"

-- Retrieval info: PRIVATE: AclrAddr NUMERIC "0"

-- Retrieval info: PRIVATE: AclrByte NUMERIC "0"

-- Retrieval info: PRIVATE: AclrData NUMERIC "0"

-- Retrieval info: PRIVATE: AclrOutput NUMERIC "0"

-- Retrieval info: PRIVATE: BYTE\_ENABLE NUMERIC "0"

-- Retrieval info: PRIVATE: BYTE\_SIZE NUMERIC "8"

-- Retrieval info: PRIVATE: BlankMemory NUMERIC "0"

-- Retrieval info: PRIVATE: CLOCK\_ENABLE\_INPUT\_A NUMERIC "0"

-- Retrieval info: PRIVATE: CLOCK\_ENABLE\_OUTPUT\_A NUMERIC "0"

-- Retrieval info: PRIVATE: Clken NUMERIC "0"

-- Retrieval info: PRIVATE: DataBusSeparated NUMERIC "1"

-- Retrieval info: PRIVATE: IMPLEMENT\_IN\_LES NUMERIC "0"

-- Retrieval info: PRIVATE: INIT\_FILE\_LAYOUT STRING "PORT\_A"

-- Retrieval info: PRIVATE: INIT\_TO\_SIM\_X NUMERIC "0"

-- Retrieval info: PRIVATE: INTENDED\_DEVICE\_FAMILY STRING "Cyclone V"

-- Retrieval info: PRIVATE: JTAG\_ENABLED NUMERIC "0"

-- Retrieval info: PRIVATE: JTAG\_ID STRING "NONE"

-- Retrieval info: PRIVATE: MAXIMUM\_DEPTH NUMERIC "0"

-- Retrieval info: PRIVATE: MIFfilename STRING "ramlpminit.mif"

-- Retrieval info: PRIVATE: NUMWORDS\_A NUMERIC "256"

-- Retrieval info: PRIVATE: RAM\_BLOCK\_TYPE NUMERIC "0"

-- Retrieval info: PRIVATE: READ\_DURING\_WRITE\_MODE\_PORT\_A NUMERIC "3"

-- Retrieval info: PRIVATE: RegAddr NUMERIC "1"

-- Retrieval info: PRIVATE: RegData NUMERIC "1"

-- Retrieval info: PRIVATE: RegOutput NUMERIC "0"

-- Retrieval info: PRIVATE: SYNTH\_WRAPPER\_GEN\_POSTFIX STRING "0"

-- Retrieval info: PRIVATE: SingleClock NUMERIC "1"

-- Retrieval info: PRIVATE: UseDQRAM NUMERIC "1"

-- Retrieval info: PRIVATE: WRCONTROL\_ACLR\_A NUMERIC "0"

-- Retrieval info: PRIVATE: WidthAddr NUMERIC "8"

-- Retrieval info: PRIVATE: WidthData NUMERIC "8"

-- Retrieval info: PRIVATE: rden NUMERIC "0"

-- Retrieval info: LIBRARY: altera\_mf altera\_mf.altera\_mf\_components.all

-- Retrieval info: CONSTANT: CLOCK\_ENABLE\_INPUT\_A STRING "BYPASS"

-- Retrieval info: CONSTANT: CLOCK\_ENABLE\_OUTPUT\_A STRING "BYPASS"

-- Retrieval info: CONSTANT: INIT\_FILE STRING "ramlpminit.mif"

-- Retrieval info: CONSTANT: INTENDED\_DEVICE\_FAMILY STRING "Cyclone V"

-- Retrieval info: CONSTANT: LPM\_HINT STRING "ENABLE\_RUNTIME\_MOD=NO"

-- Retrieval info: CONSTANT: LPM\_TYPE STRING "altsyncram"

-- Retrieval info: CONSTANT: NUMWORDS\_A NUMERIC "256"

-- Retrieval info: CONSTANT: OPERATION\_MODE STRING "SINGLE\_PORT"

-- Retrieval info: CONSTANT: OUTDATA\_ACLR\_A STRING "NONE"

-- Retrieval info: CONSTANT: OUTDATA\_REG\_A STRING "UNREGISTERED"

-- Retrieval info: CONSTANT: POWER\_UP\_UNINITIALIZED STRING "FALSE"

-- Retrieval info: CONSTANT: READ\_DURING\_WRITE\_MODE\_PORT\_A STRING "NEW\_DATA\_NO\_NBE\_READ"

-- Retrieval info: CONSTANT: WIDTHAD\_A NUMERIC "8"

-- Retrieval info: CONSTANT: WIDTH\_A NUMERIC "8"

-- Retrieval info: CONSTANT: WIDTH\_BYTEENA\_A NUMERIC "1"

-- Retrieval info: USED\_PORT: address 0 0 8 0 INPUT NODEFVAL "address[7..0]"

-- Retrieval info: USED\_PORT: clock 0 0 0 0 INPUT VCC "clock"

-- Retrieval info: USED\_PORT: data 0 0 8 0 INPUT NODEFVAL "data[7..0]"

-- Retrieval info: USED\_PORT: q 0 0 8 0 OUTPUT NODEFVAL "q[7..0]"

-- Retrieval info: USED\_PORT: wren 0 0 0 0 INPUT NODEFVAL "wren"

-- Retrieval info: CONNECT: @address\_a 0 0 8 0 address 0 0 8 0

-- Retrieval info: CONNECT: @clock0 0 0 0 0 clock 0 0 0 0

-- Retrieval info: CONNECT: @data\_a 0 0 8 0 data 0 0 8 0

-- Retrieval info: CONNECT: @wren\_a 0 0 0 0 wren 0 0 0 0

-- Retrieval info: CONNECT: q 0 0 8 0 @q\_a 0 0 8 0

-- Retrieval info: GEN\_FILE: TYPE\_NORMAL ramlpminit.vhd TRUE

-- Retrieval info: GEN\_FILE: TYPE\_NORMAL ramlpminit.inc FALSE

-- Retrieval info: GEN\_FILE: TYPE\_NORMAL ramlpminit.cmp TRUE

-- Retrieval info: GEN\_FILE: TYPE\_NORMAL ramlpminit.bsf TRUE

-- Retrieval info: GEN\_FILE: TYPE\_NORMAL ramlpminit\_inst.vhd TRUE

-- Retrieval info: LIB\_FILE: altera\_mf

**Demux2.vhd**

library ieee;

use ieee.std\_logic\_1164.all;

entity demux2 is

port(

data: in std\_logic\_vector(7 downto 0);

s: in std\_logic;

address: out std\_logic\_vector(7 downto 0);

value\_out: out std\_logic\_vector(7 downto 0)

);

end demux2;

architecture behav of demux2 is

begin

process(data, s)

begin

--load address

if (s = '0') then

address <= data;

elsif (s = '1') then

value\_out <= data;

end if;

end process;

end behav;

### Do Code

**lab6\_ramlpinit\_sim.txt**

add wave -in \*

add wave -out \*

restart -f

force clk 0 0ns, 1 20ns -r 40ns

force wren 0

force address x"00"

run 40ns

force address x"01"

run 40ns

force address x"02"

run 40ns

force address x"03"

run 40ns

force address x"04"

run 40ns

force address x"05"

run 40ns

force address x"06"

run 40ns

force address x"07"

run 40ns

force address x"08"

run 40ns

force address x"09"

run 40ns

force address x"0A"

run 40ns

force address x"0B"

run 40ns

force address x"0C"

run 40ns

force address x"0D"

run 40ns

force address x"0E"

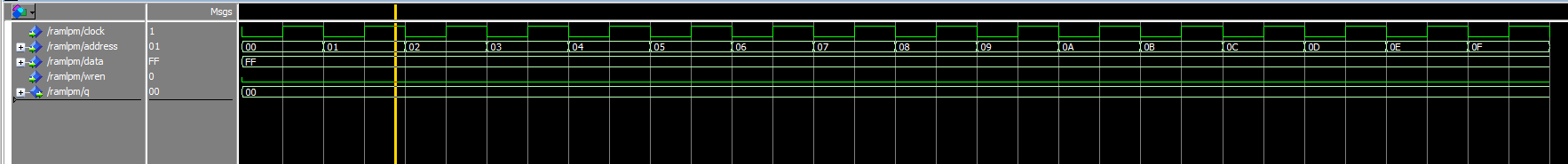
run 40ns

force address x"0F"

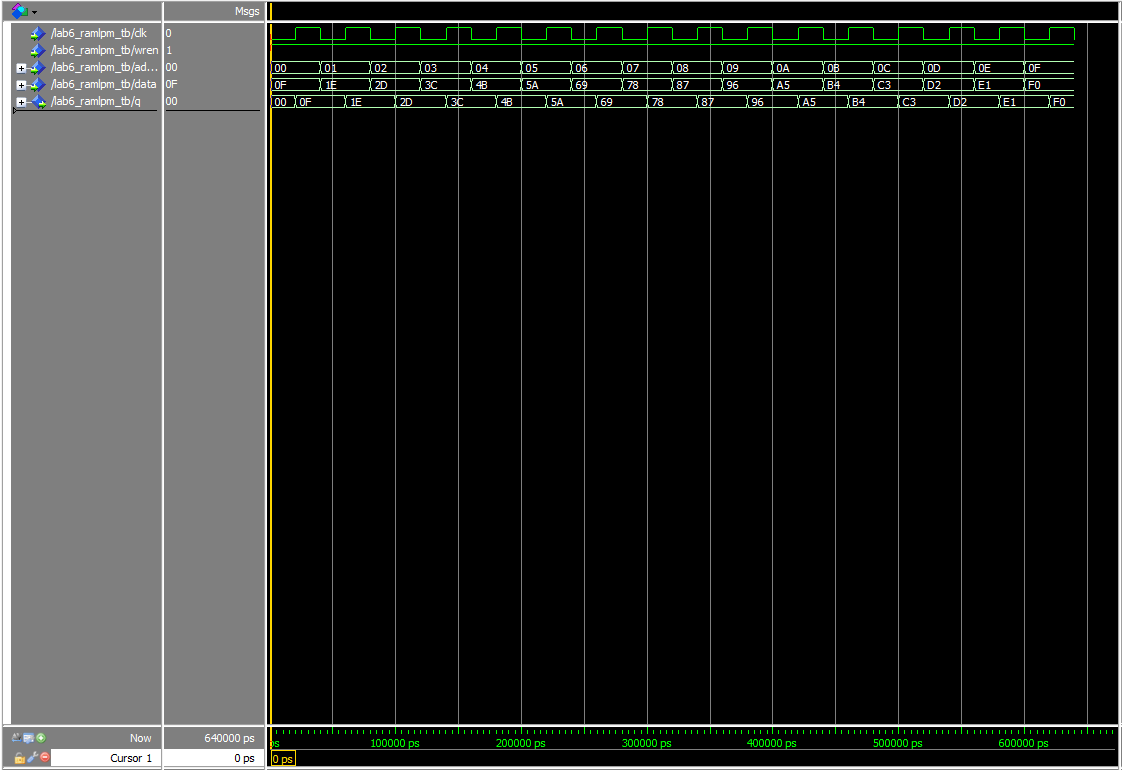
run 40ns

## Screenshots

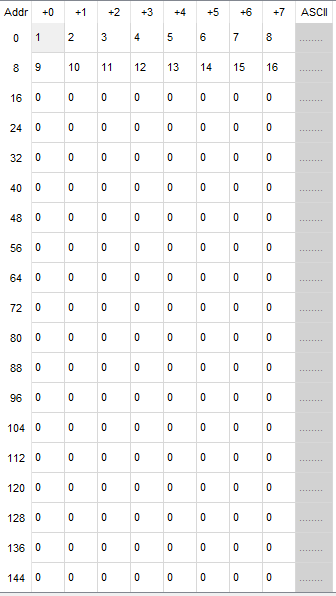
**Activity 1: Part 1: First 16 addresses’ initial values**

****

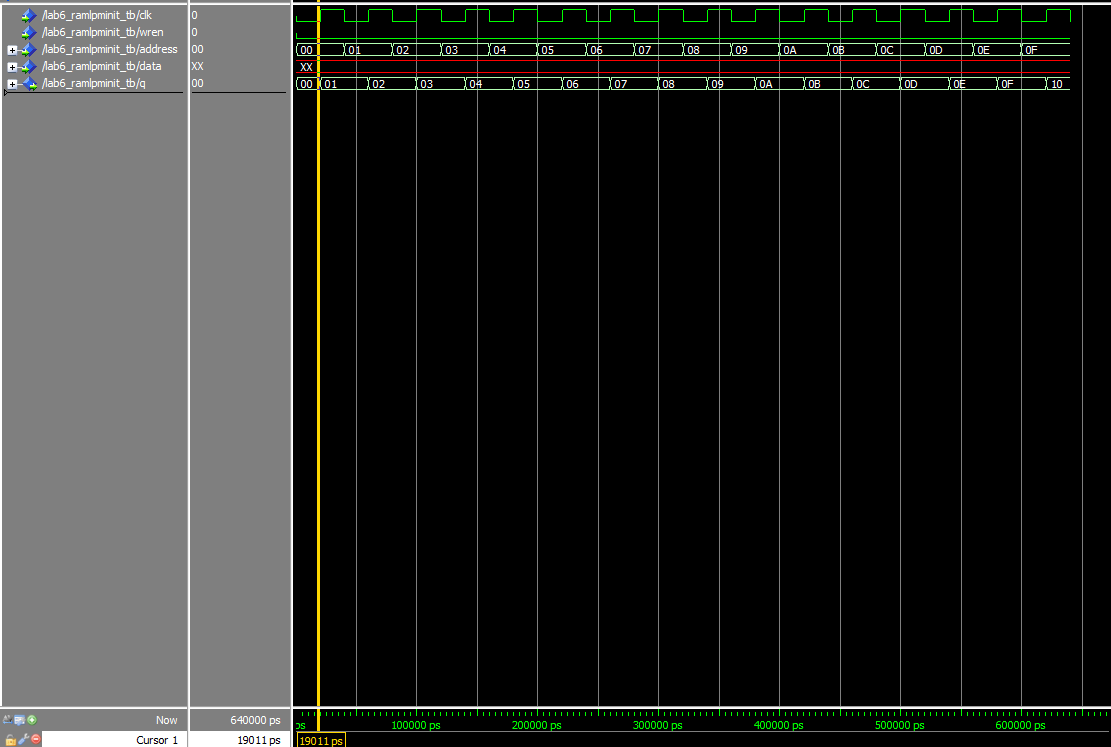
**Activity 1: Part 2: Read/write test**

****

**Activity 2: mif file**



**Activity 2: ramlpminit.vhd sim**



## Conclusion

This was a great lab! It was easy going and we encountered very little errors. Looking forward to lab 7.